iFVTX Update

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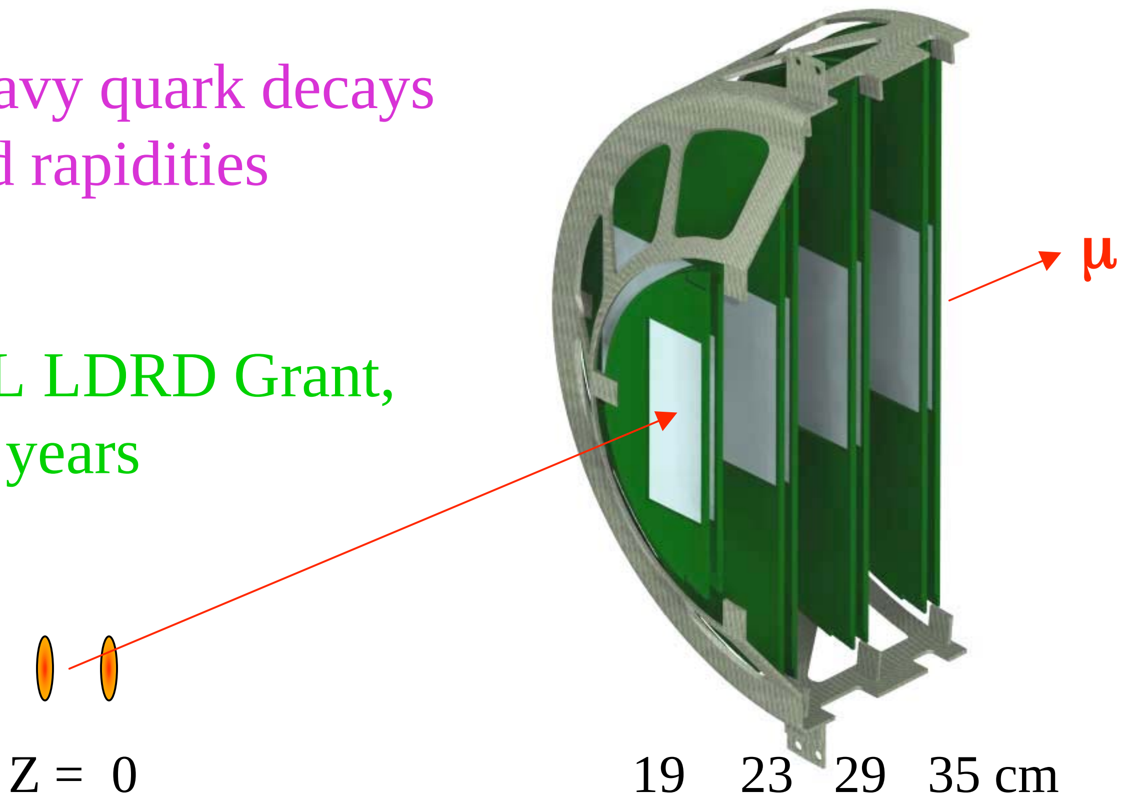
Goal : Detect heavy quark decays
at forward rapidities

Supported by LANL LDRD Grant,
~1.25 M$ / yr for 3 years



PHENIX DC Meeting 1/10/07

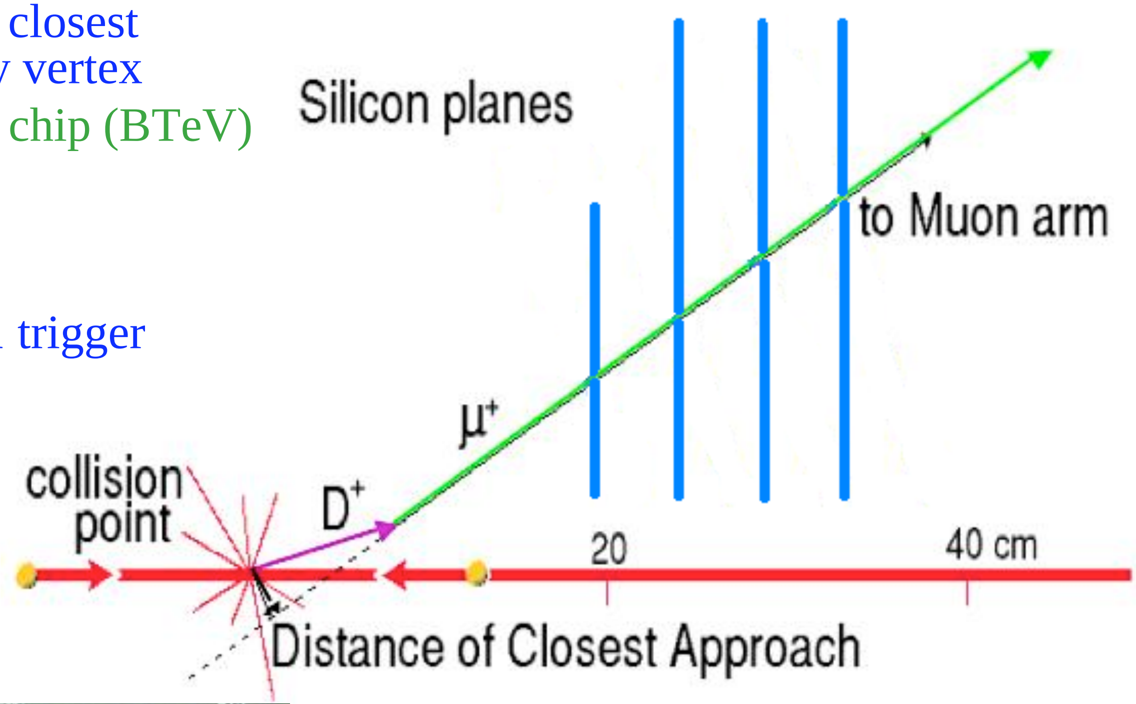
Pixel-based iFVTX

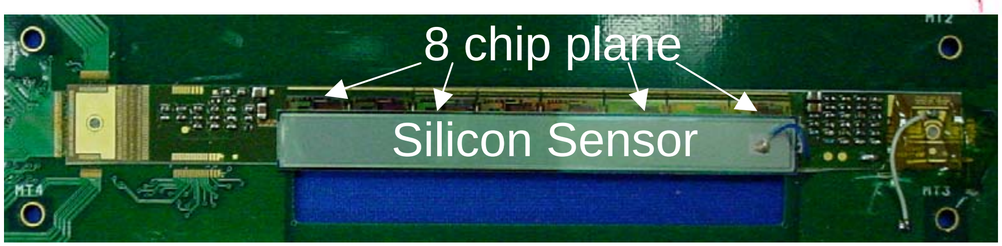
- LANL/ FNAL/ Columbia / UNM/ NMSU / ISU collaboration
- Designed to measure distance of closest approach of tracks to the primary vertex
- 4 planes of pixel tiles with FPIX chip (BTeV) bump bonded to a Silicon sensor
- Provides a DCA resolution of σ_{DCA} ~ 100-200 microns
- Can send data to prototype Lvl-1 trigger boards

Measures :

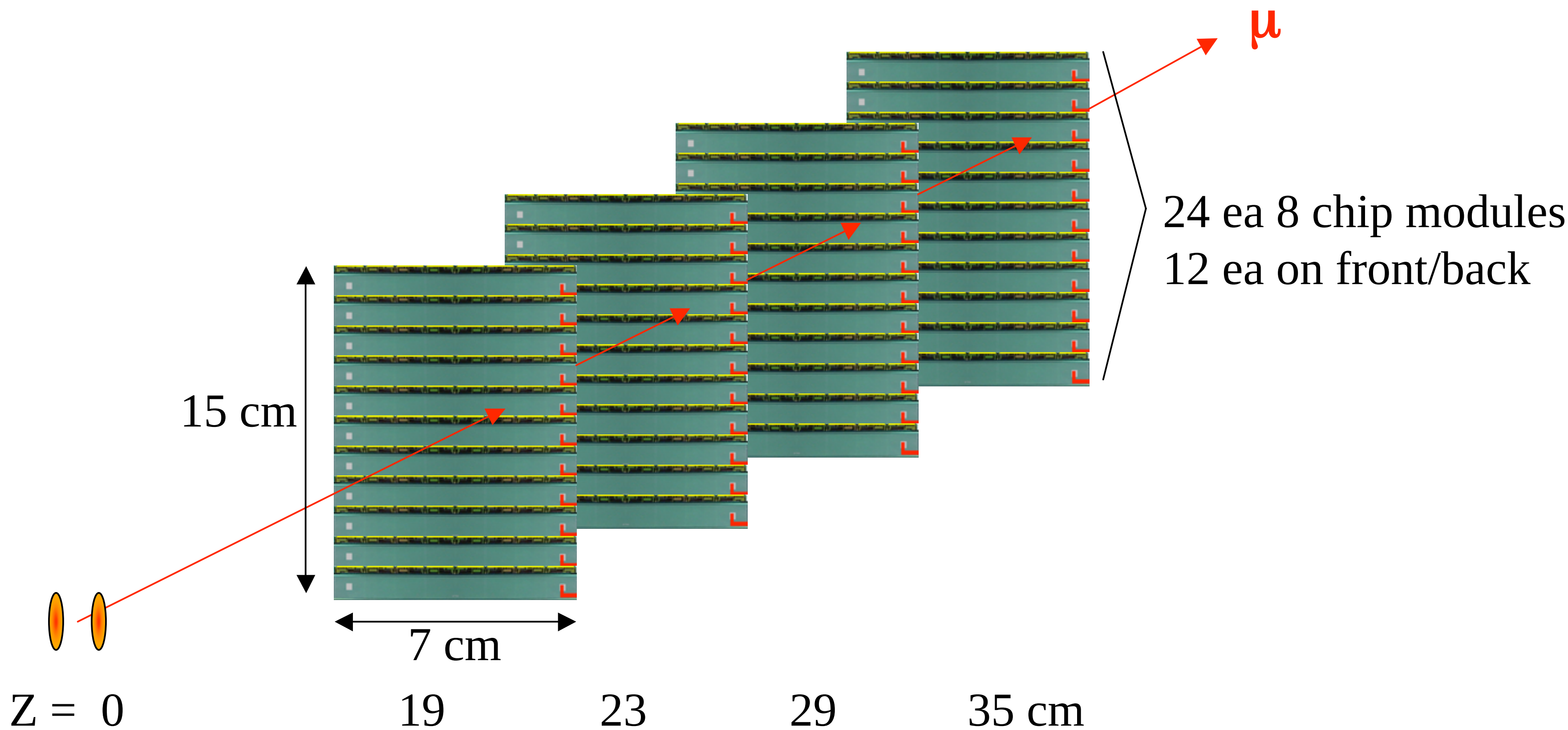
D (charm) → μ + X

B (beauty)→ μ + X





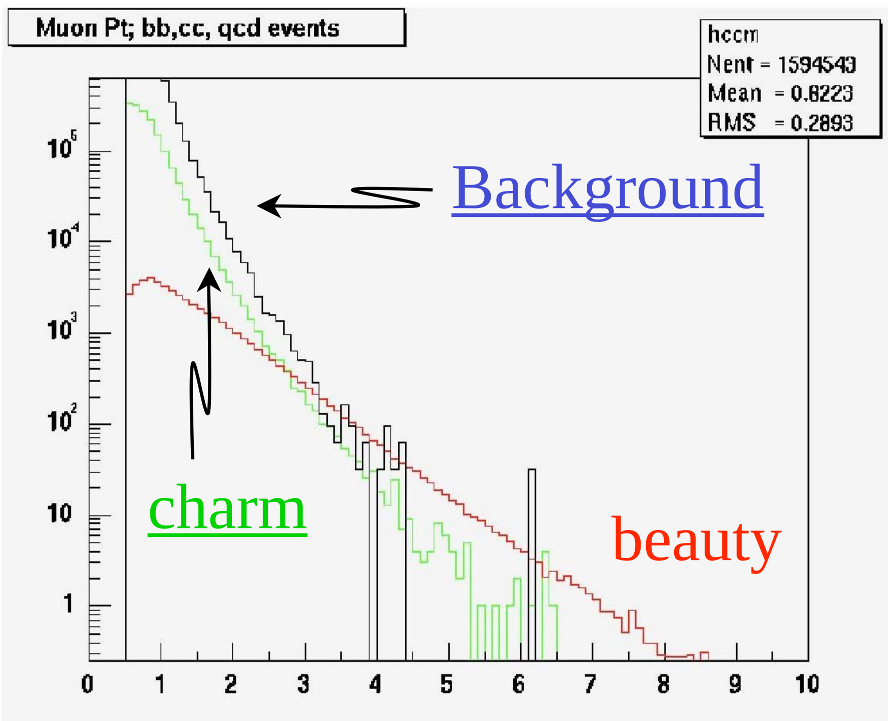
iFVTX Detector Planes



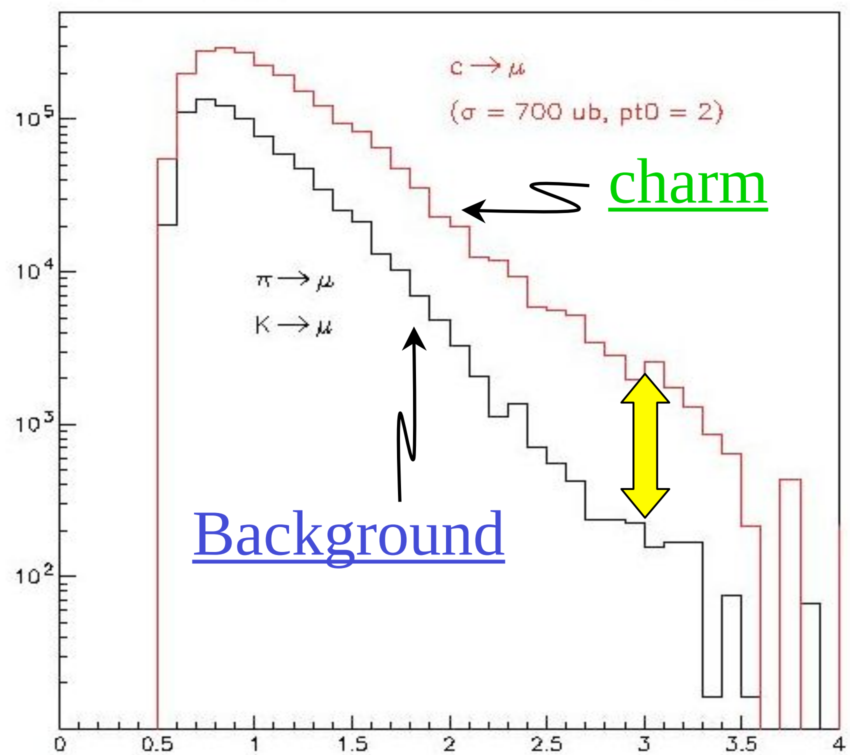
- 4 Tracking stations composed of Si pixels, 50 by 400 um
- Cover ~ 1/8 of one muon arm (one octant) with ~100 detector modules
- Electronics recently developed by FNAL for BTeV, ~2M pixels.
  Low power, high speed and high resolution pixel detector.
- Can detect large numbers of D and some B decays per year at RHIC.

Dramatic Signal / Background Improvement for Heavy Quarks

Before vertex cuts Muon Events After vertex cuts



p_T (GeV/c)



p_T (GeV/c)

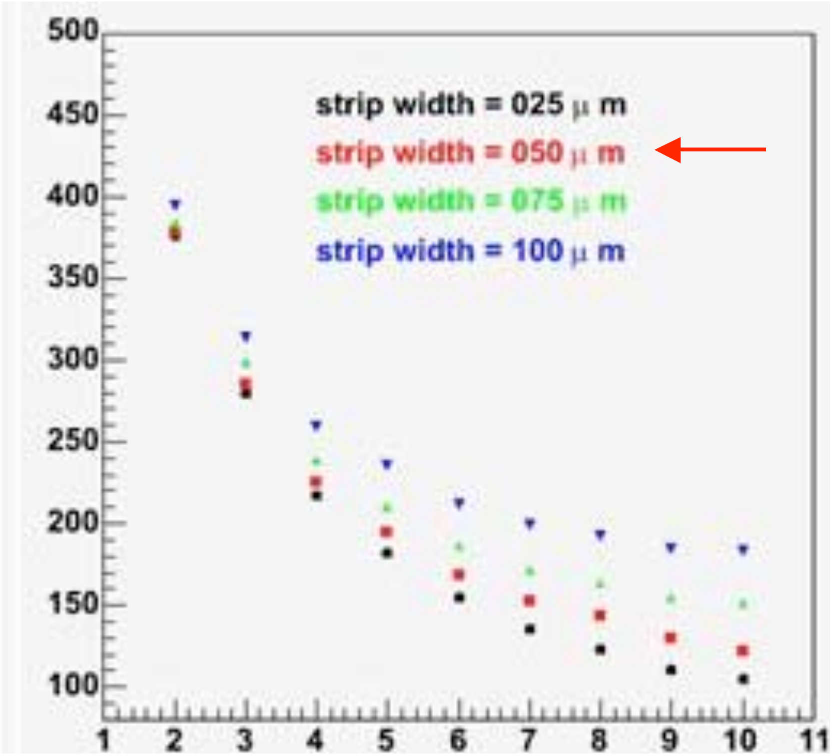
Simulated Signal to Noise for D→ μ+X without and with vertex cuts, 10 X improvement in signal / background → accurate yield, slope of charm

Heavy Quark Yields*, for 1/8 of a Muon Arm

Run	Ions	Luminos. on tape	D $\rightarrow \mu$ triggered counts	B $\rightarrow \mu$ triggered counts	B$\rightarrow$J/$\psi \rightarrow \mu$ with 1 μ in SiVTX
2007	p+p	67 pb^{-1}	$28*10^6$	$24*10^3$	240
2008	Au+Au	760 ub^{-1}	$8*10^6$	$6*10^3$	160

- *Rates before application of a vertex cut.

Z-Vertex Resolution, μm



Muon Momentum, GeV

iFVTX Status - Detector Elements

- Silicon Pixel Detectors
  - Total 28 wafers (6 detectors per wafer) fabricated by CIS, tested at CIS and UNM. More than enough for iFTX + spares
  - Excellent yields (~93%), only 1 bad wafer from 1st 20.
- Front End Chip (FPIX2)
  - Total 11 wafers produced by MOSIS / TSMC.
  - 1 wafer tested, good yield (~77%). Should have plenty of good die. Testing underway.
- Flip Chip Assembly of Detector Modules (Bump Bonding)
  - ~30 prototype multi-chip modules delivered from VTT.
  - Testing underway, yield low due to use of untested FPIX chips.
  - Will submit pre-production parts to VTT soon.
- High Density Interconnect (Kapton bus)
  - Prototypes delivered from CERN are OK, but yield was poor.
  - Have re-designed a simpler HDI, first deliveries mid Jan.

iFVTX Status - Mechanical

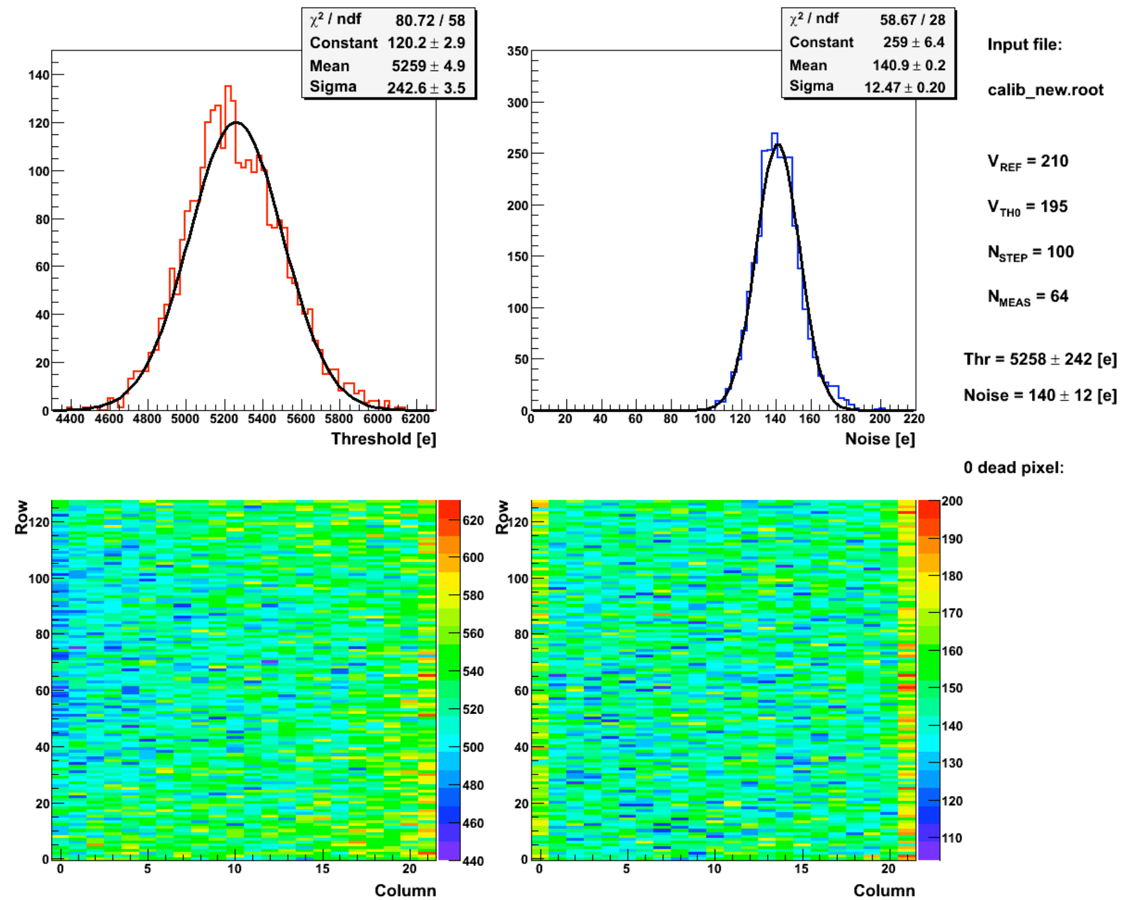
- Picture Frame (Detector Plane PC Board)
  - Prototype being designed at FNAL, uses TPG to transfer heat to liquid cooling.
  - Thermal issues have been studied, appropriate glues selected
- Mechanical Support Structure
  - Design underway at HYTEC.
  - Will fit into same cage design as FVTX and not interfere with VTX.
- Cooling System
  - Haven’t chosen coolant temperature yet, may want detector to operate at room temperature.
  - Heat load should not be a problem (FPIX $<$ 200 W).
- FPIX / Sensor Modules
  - Plan to assemble and test at FNAL.

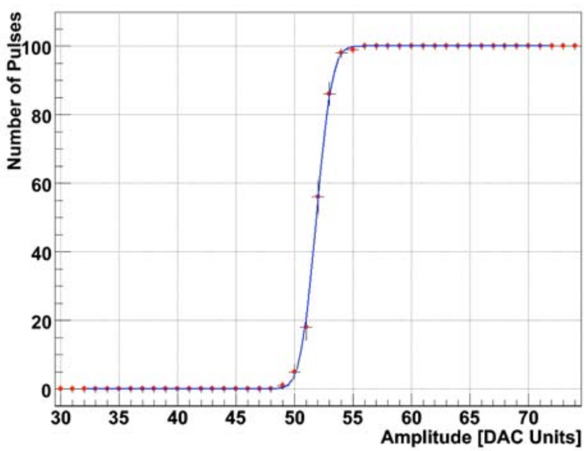
iFVTX Status - DAQ

- Pixel Module Test Stand
  - FPGA/PCI readout card and software are working.
- Calibration and monitoring
  - Pulse injection system prototyped and working.
  - Current, voltage and temperature monitor working.
- Columbia/Nevis DAQ approach :
  - FPGA at detector receives data driven FPIX output, sends to counting house over fiber.
  - Receiver on PCI card in PHENIX DAQ farm uses DMA to put selected data into event memory.
  - Prototype system tested and working with standalone PC.
- LANL approach : ROC, FEM and DCM
  - Read Out Controller has FPGA at detector, sends data to :
  - Front End Module selects triggered event data, sends data to standard PHENIX DCM.
  - ROC and FEM prototypes working with interface to PC, no fiber interface yet.

LANL FPIX2.1 / sensor Calibration Results

- Realistic triggered readout.
- Results of threshold scan reproduce FNAL test results. ➔
  - **The proposed readout design is working as expected**
- 7 min required for 100 pulses at 64 amplitude settings.
- One pixel tested at a time, Measured noise is 140 electrons!





Hardware Completion Schedule

• FY06 :	HDI designed	done
	First pixel modules flip chip assembled	done
	Si sensors delivered	done
	FPIX2.1 readout chips delivered	done
	Test bench DAQ systems	done
• FY07 :	Decision on DAQ design	03/07
	HDI Production	05/07
	Flip chip Si detectors and FPIX readout chips	08/07
	Beam test of a few modules	???
• FY08 :	Pixel plane printed circuit boards	10/07
	Pixel module assembly	03/08
	DAQ Electronics	03/08
	Pixel plane assembly	06/08
• FY09 :	Full system testing outside of PHENIX	12/08
	Ready for installation in PHENIX, needs VTX for primary vertex determination. Useful with p-p, d-Au or Au-Au beams	

Benefits to FVTX Program

- Expect to use same readout design and test stands for iFVTX and FVTX.

- Share same mechanical support structure with FVTX, with one additional insert for iFVTX. Can be assembled independently of VTX, FVTX.

- Simulation and analysis tools developed for iFVTX work for FVTX as well. Mainly a change in the length of the pixels.

- Experience gained with hit rates, noise levels, etc will provide useful input for FVTX program.

- Several man-years of R+D work are being paid by our LDRD grant, much of which is of direct value to the FVTX.

Next Steps with PHENIX ?

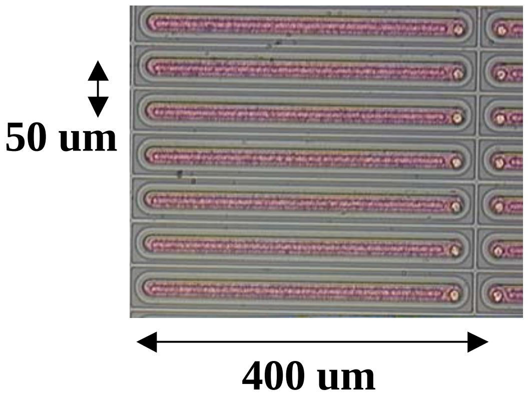
- Letter of intent.
- Timing of installation with respect to HBD, VTX, FVTX.
- Required PHENIX DAQ resources and systems integration.
- What else ?

Backup slides

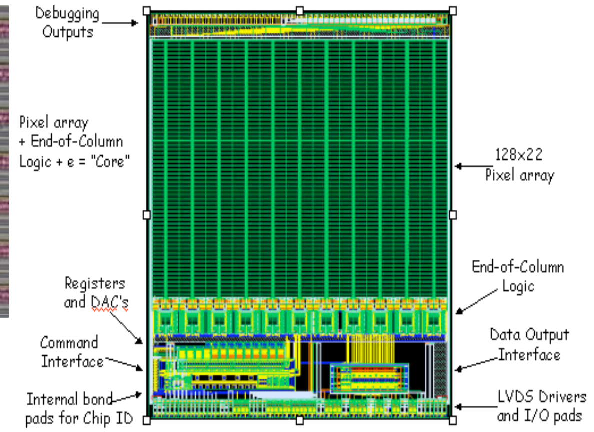
BTeV Pixel Detector Module

- **Pixel Sensor bump-bonded to Readout chip**
- **Fine segmentation**
  - **50 μm x 400 μm**
  - **Large number of channels**
  - **Electronics in the active tracking volume**
  - **High power density**
    → cooling system required
- **Basic building block – Multichip Module (MCM)**
  - **8 readout chips / module**
  - **HDI and flex cables**
- **Assemble modules on both sides of substrate to form pixel plane; providing a high resolution radius measurement plus a good phi measurement.**

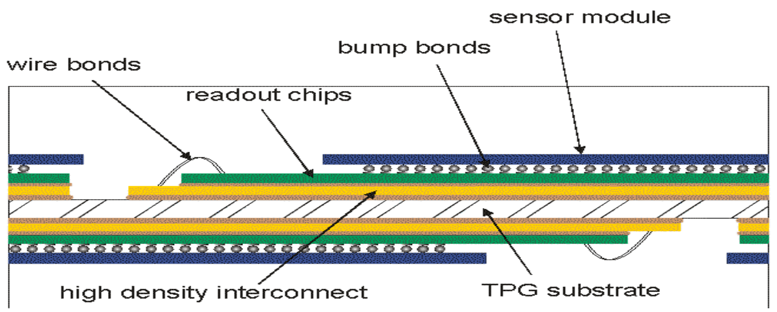
Si pixel sensors



FPIX 2 Pixel Readout chip

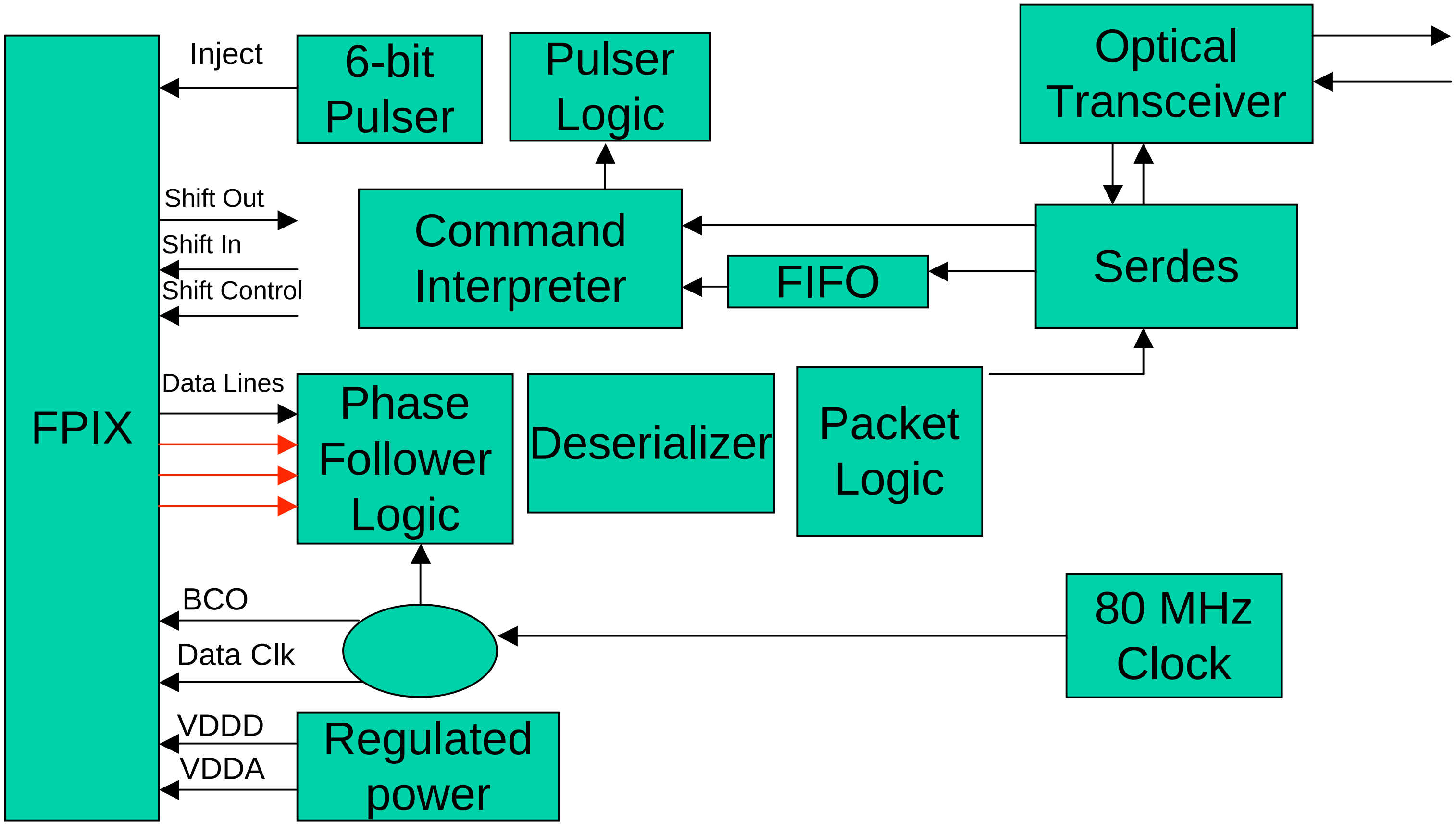


Multichip module



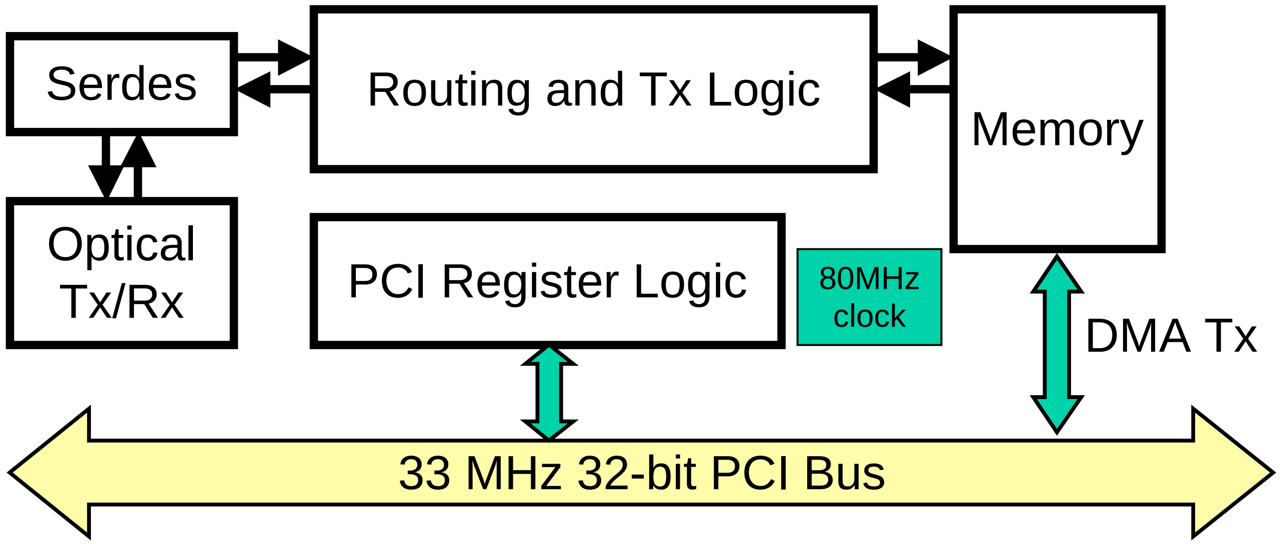
Module Assembly

Nevis FPIX Interface



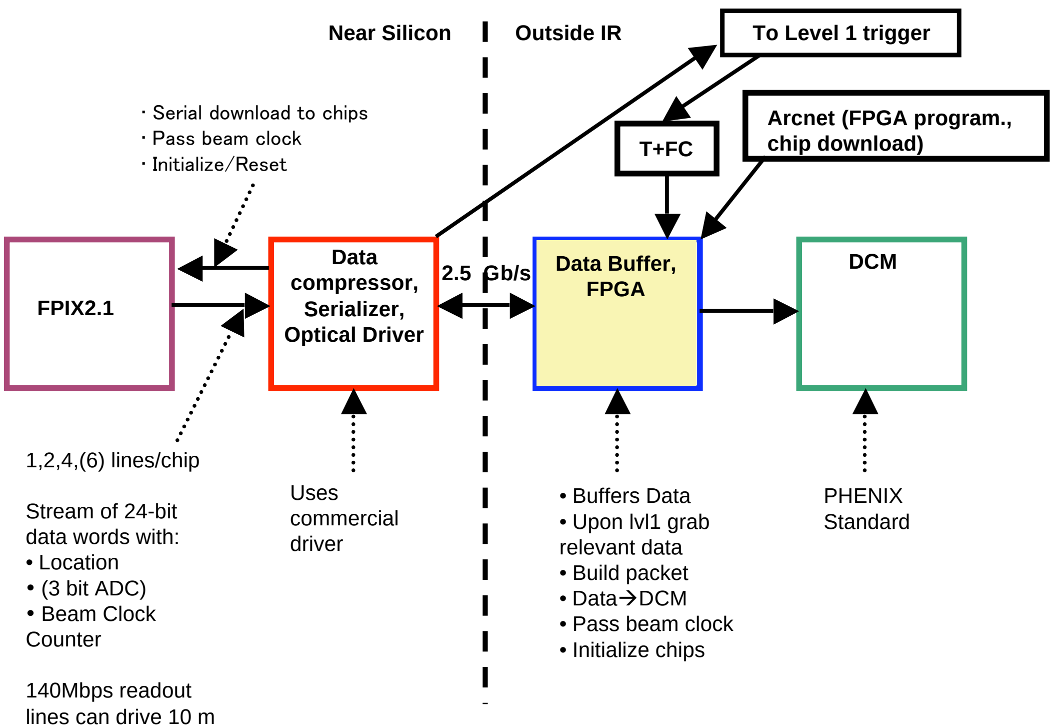
- Current design reads single FPIX with 1- or 4-lines
- Altera Cyclone FPGA
- No provision for time-ordering pixel data
- Includes 15-bit counter to implement timed commands and timestamps
- FIFO buffers non-immediate commands (128 deep)

Nevis FPIX Receiver



- Implemented as 32-bit 33 MHz PCI card
- Provides 3 channels: Control out, control in, data in
- Communicates with user via registers
- Dataflow governed by ABC register architecture (one set of ABC per channel)
  - A : physical RAM address (in PC) of next DMA transfer
  - B : physical RAM address (in PC) of next user access
  - C: contains bookkeeping to allow pci card to know when/where to wrap A values
- Uses ACEX family FPGA
- 256 kB SRAM on-board

LANL Pixel Detector Readout Design



- Readout electronics split into two parts
  - Near the detector
    - Compresses and serializes the data from a group of chips
    - Radiation tolerance ➔ use FLASH based FPGAs from Actel
    - Fiber link to the control room
  - In the Control Room (FEM)
    - Buffer data for 64 beam clocks
    - Write data upon LVL1 trigger request
    - SRAM based FPGAs from Xilinx (Altera)

FNAL Readout Chip Comparison

Chip All 50 μm spacing	Noise Threshold σ	Ministrip	Readout type speed	Trigger possible	Power per chan	Geometry r-phi
SVX4 128 ch	S/N -12/1	yes	Pipeline 53 MHz	no	2 mW	yes
FSSR 128 ch	250 e 440 e	yes	Data push 840 Mb	yes	3 mW	yes
FPIX 2816 ch	220 e 125 e	no	Data Push 840 Mb	yes	90 μW	no

FSSR and FPIX chip are good candidates for LDRD project

Signal = 24000 e for 300 μm Si Sensor.